# Large Area Graphene Field Effect Devices with Sputtered Nitride and Oxide Top-Dielectrics

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Realizing high-speed (high $f_t$) graphene transistors requires the high capacitance of a thin top-gated dielectric structure. The deposition of a top-gate dielectric can significantly reduce mobility due an increased density of trapped charges [1] and damage to the graphene during the deposition process. However, high-$\kappa$ dielectrics such as ionic liquids have been observed to enhance mobility [2], explained by dielectric screening of charged impurities. The effect of a dielectric on mobility remains not fully understood [3,4]. Moreover, a graphene field effect device is doped by adsorbates according to the chemical nature of the dielectric surface in contact with the graphene [5]. We report an experimental study on the field effect mobility and doping of large area graphene field effect devices encapsulated by two top-layer dielectrics: $SiO_2$ ($\varepsilon_r$~3.9) and $Si_3N_4$ ($\varepsilon_r$~3.9) grown by magnetron sputter deposition.

Graphene was grown on Cu foils in a tube furnace with a methane/hydrogen gas mixture at a growth temperature of 900°C. The graphene was transferred to insulating substrates using a poly(methyl methacrylate) (PMMA) handle and sacrificial etch of the Cu in ammonium persulfate (0.1M). Further details of the growth and transfer process are described elsewhere [6,7]. Heavily doped Si (n-doped, 8-20 mΩ-cm) with 300 nm of dry, chlorinated thermal $SiO_2$, was chosen as the substrate for back-gated electrical measurements. Standard photolithography, electron beam evaporation and lift-off techniques were used to define Ohmic contacts (10nm Ti/100nm Au). Subsequent photolithography and oxygen plasma treatment was used to isolate graphene sheets in a 4-point van der Pauw geometry (Fig. 1).

Raman spectroscopy at a 514.5nm pump wavelength was used to characterize the graphene before and after deposition of a top-side dielectric. The sheet resistance $R_S$ was measured by the van der Pauw technique as a function of back gate voltage $V_{GS}$. All electrical measurements were performed in a variable environment probe station following a 400K, $10^{-5}$Torr anneal over a minimum of 12 hours. Sheet resistance measurements were taken before and after deposition of a top-side dielectric. Magnetron sputtering with a Si target and RF plasma source was used to deposit 10nm of $SiO_2$ (20sccm of Ar and $O_2$ gas at 5mbar, 20nm/min growth rate) or 10nm of $Si_3N_4$ (25sccm of Ar and $N_2$ gas at 5mbar, 3.3nm/min growth rate).

Raman spectroscopy reveals an increase in D-peak (~1350cm$^{-1}$) intensity following deposition of either dielectric, as well as an increase in background fluorescence (Fig. 2). The origin of the fluorescence is possibly due to plasma induced damage of graphene during sputtering [8]. Sheet resistance $R_S$ versus back gate voltage $V_{GS}$ measurements (Fig. 3) reveal that both $SiO_2$ and $Si_3N_4$ top-dielectric layers significantly reduce the doping of the field effect transistors, presumably due to the reduced presence of water [5]. The carrier mobility, $\mu = [CR_S(V_{GS}-V_{NP})]^{-1}$ where C = 11.8nF/cm$^2$ is the back-gate capacitance and $V_{NP}$ is the neutrality point back-gate voltage, was compared at an electron density n = $10^{12}$/cm$^2$ for a series of devices before and after deposition of top-gate dielectrics (Fig. 4). Carrier mobilities as high as ~2000cm$^2$/Vs were achieved with a top-dielectric. Our results are comparable to that of microscopic exfoliated graphene samples encapsulated with nitride by chemical vapour deposition [9]. In several devices, a minimal change in mobility was observed before and after $Si_3N_4$ deposition. Future work to incorporate top-gated large-area graphene devices in high-frequency compatible structures is underway.

## References


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## Figures

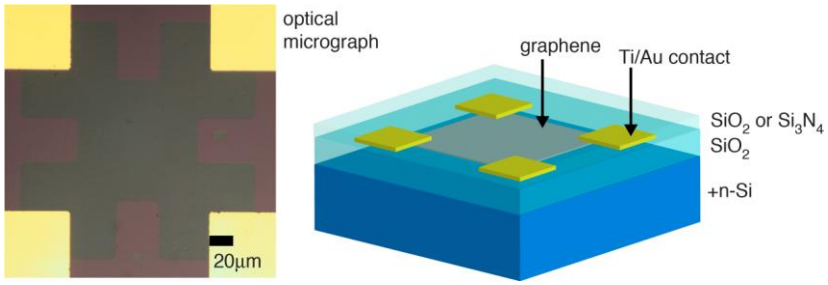


*Fig. 1 : Graphene is transferred, etched and contacted into a van der Pauw sample on a $SiO_2$/Si substrate for back gating. A dielectric top layer of 10nm $SiO_2$ or 10nm $Si_3N_4$ is sputtered for encapsulation.*

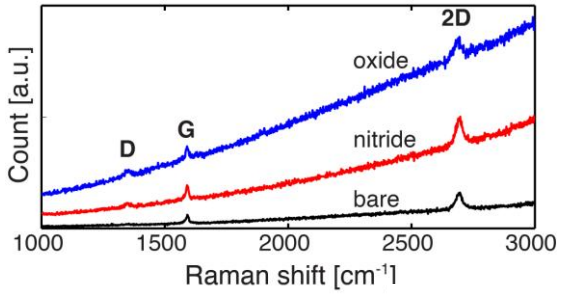


*Fig. 2 : Raman spectra (λ=514.5nm) of large area graphene as transferred to $SiO_2$/Si. Following deposition of a $Si_3N_4$ dielectric top layer, an increase in D-peak (~1350cm$^{-1}$) scattering and background fluorescence is observed. A more intense D-peak and greater background fluorescence is observed with $SiO_2$ deposited as a dielectric top layer.*

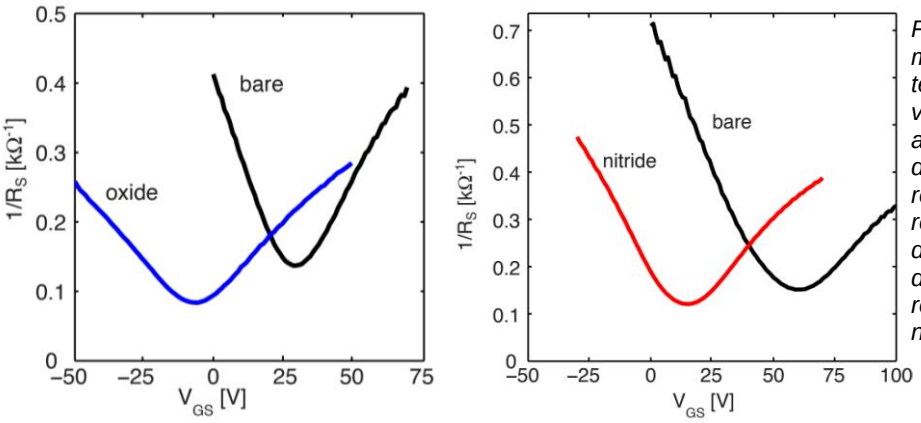


*Fig. 3 : Sheet resistance $R_S$ measured by van der Pauw technique versus back-gate voltage $V_{GS}$. A device before and after $SiO_2$ top-dielectric deposition (left) shows a reduction in doping and a reduction in mobility. A device before and after $Si_3N_4$ deposition (right) shows a reduction in doping and a negligible change in mobility.*

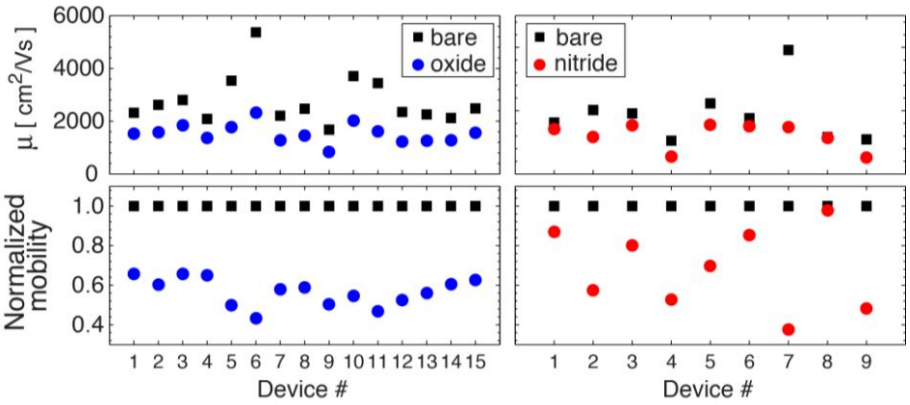


*Fig. 4 : Carrier mobility μ at electron density n = $10^{12}$/cm$^2$ inferred from $R_S$ versus $V_{GS}$. The mobility is compared before and after dielectric deposition. The mobility normalized to that of the bare device before deposition is also compared. In several cases, a minimal change in mobility is observed.*